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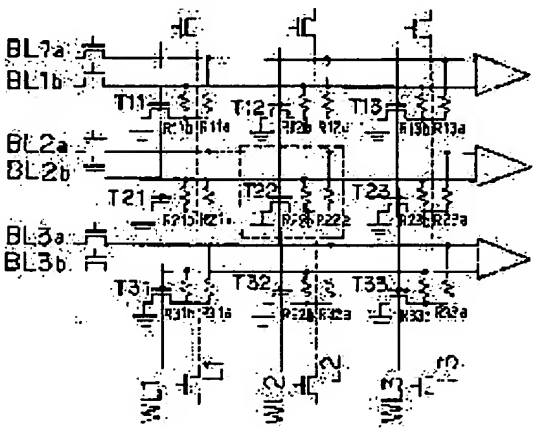
(54) FERROMAGNETIC NON-VOLATILE STORAGE ELEMENT, ITS INFORMATION REPRODUCING METHOD, MEMORY CHIP USING IT, AND PORTABLE INFORMATION PROCESSING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a ferromagnetic non-volatile storage element in which cell area can be reduced, storage information can be detected at high speed and accurately even if a magnetic resistance variation rate is small, and can be integrated in high density.
SOLUTION: A unit cell constituting a memory of one bit is constituted of two magnetic resistance elements R22a, R22b magnetized so that respective direction of magnetization is reverse direction, and one semiconductor switch element T22 for selecting these magnetic resistance elements. In the semiconductor switch element, a drain terminal is connected commonly to one side of terminals of the magnetic resistance elements R22a, R22b, a source terminal is connected to ground, and a gate terminal is connected to a word line WL2. Other terminals of the magnetic resistance elements R22a, R22b are connected to bit lines BL1a, BL1b respectively.



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CLAIMS

[Claim(s)]
[Claim 1] The ferromagnetic non-volatile storage element characterized by the unit cell which constitutes 1-bit memory consisting of the 1st and 2nd magnetic resistance elements magnetized so that the sense of mutual magnetization may turn into reverse sense, and one solid state switch component for choosing these 1st and 2nd magnetic resistance elements.
[Claim 2] Said solid state switch component is connected common [a drain terminal] to one [each] terminal of said 1st and 2nd magnetic resistance elements. A source terminal is grounded, and it is constituted so that these drain terminal and a source terminal may be electrically connected by a predetermined electrical potential difference being impressed to a gate terminal. The 1st and 2nd bit line to which the other-end child of said 1st and 2nd magnetic resistance element was connected, respectively, The ferromagnetic non-volatile storage element according to claim 1 characterized by having further the sense amplifier which compares the electrical-potential-difference value according to the magnetization condition of said 1st and 2nd magnetic resistance elements produced in said 1st and 2nd bit lines.
[Claim 3] The ferromagnetic non-volatile storage element according to claim 2 characterized by connecting one terminal of said 1st and 2nd magnetic resistance element to the drain terminal of said solid state switch component through diode, respectively.
[Claim 4] Said 1st and 2nd magnetic resistance element is equipped with the 1st [which has an easy axis], and 2nd ferromagnetic film in the predetermined direction, respectively. Said a part of 1st bit line is located in right above [of said 1st ferromagnetic film]. Said a part of 2nd bit line is located in right above [of said 2nd ferromagnetic film]. It has further write-in wiring which passes directly under said 1st and 2nd ferromagnetic film. While said 1st ferromagnetic film is magnetized in the predetermined direction in accordance with an easy axis by the magnetic field which produces the current of predetermined magnitude by passing in the predetermined direction to the both sides of said 1st bit line and write-in wiring By the magnetic field which produces the current of predetermined magnitude by passing in the predetermined direction to the both sides of said 2nd bit line and write-in wiring The ferromagnetic non-volatile storage element according to claim 2 characterized by being constituted so that said 2nd ferromagnetic film may be magnetized in the predetermined direction in accordance with an easy axis.
[Claim 5] The ferromagnetic non-volatile storage element according to claim 1 characterized by said 1st and 2nd magnetic resistance elements consisting of tunnel magnetic resistance elements.
[Claim 6] The ferromagnetic non-volatile storage element according to claim 5 with which the ferromagnetic film which constitutes said tunnel magnetic resistance element is characterized by being horizontally magnetized to membranous field inboard.
[Claim 7] The ferromagnetic non-volatile storage element according to claim 5 with which the ferromagnetic film which constitutes said tunnel magnetic resistance element is characterized by being perpendicularly magnetized to membranous field inboard.
[Claim 8] Said 1st and 2nd magnetic resistance elements are ferromagnetic non-volatile storage elements according to claim 1 characterized by being arranged adjacently.
[Claim 9] The ferromagnetic non-volatile storage element according to claim 1 characterized by said solid state switch component being the field effect transistor which has the channel field which made SiGe the subject.
[Claim 10] The ferromagnetic non-volatile storage element according to claim 1 characterized by the substrate with which said solid state switch component is formed being a SOI substrate.

[Claim 11] The 1st and 2nd magnetic resistance element magnetized so that the sense of mutual magnetization connected to the 1st and 2nd bit line with which a predetermined electrical potential difference is supplied, respectively may turn into reverse sense, It is the information playback approach of a ferromagnetic non-volatile storage element that the unit cell which constitutes 1-bit memory from one solid state switch component for choosing these 1st and 2nd magnetic resistance elements is constituted. The 1st electrical-potential-difference value of said 1st bit line which chooses said 1st and 2nd magnetic resistance elements by making said solid state switch component into an ON state, and is produced according to the magnetic-reluctance value of the 1st this chosen magnetic resistance element, the 2nd electrical-potential-difference value of said 2nd bit line produced according to the magnetic-reluctance value of the 2nd this selected magnetic resistance element -- comparing -- electrical-potential-difference value [of ** a 1st] > -- the case of the 2nd electrical-potential-difference value -- the 1st information -- carrying out -- the 1st electrical-potential-difference value -- < -- the information playback approach characterized by reading the case of the 2nd electrical-potential-difference value as the 2nd information.

[Claim 12] The memory chip by which the ferromagnetic non-volatile storage element given in either of claims 1-10 was formed on the semi-conductor substrate.

[Claim 13] The memory chip according to claim 12 by which the control circuit which performs writing of the information in said ferromagnetic non-volatile storage element and control of read-out was formed on the same substrate.

[Claim 14] The pocket mold information processor characterized by having the program storing memory which becomes either of claims 1-10 from the ferromagnetic non-volatile storage element of a publication, and the control means which operates according to the program stored in this program storing memory.

[Claim 15] The pocket mold information processor according to claim 14 characterized by controlling transmission and reception of the information have further the means of communications which can transmit and receive the information through a wire circuit or a wireless circuit, and said control means minded said means of communications.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the non-volatile storage element using a ferromagnetic about a storage element. Furthermore, it is related with the memory chip and pocket mold information processor using such a storage element.
[0002]
[Description of the Prior Art] Generally, the ferromagnetic has the property (this is called residual magnetization) that the magnetization generated in the ferromagnetic by the magnetic field impressed from the outside remains also after removing an external magnetic field. Such a ferromagnetic has the so-called magneto-resistive effect from which electric resistance changes with the direction of magnetization, the existence of magnetization, etc. as an ingredient with a big magneto-resistive effect -- a huge magnetic-reluctance (GMR;Giant Magneto-Resistance) ingredient -- there is overly a huge magnetic-reluctance (CMR;Colossal Magneto-Resistance) ingredient, and all consist of a metal, an alloy, a multiple oxide, etc. Nonvolatile memory (memory which does not lose storage even if it turns off the power) can consist of using the electric resistance value change by selection of such a magnetization direction of a magnetic-reluctance ingredient, and the existence of magnetization. This is the so-called magnetic memory (MRAM;Magnetic Random Access Memory).
[0003] Many of MRAM(s) to which development is advanced recently have taken the method which changes and reads change of the reluctivity produced by the difference in the magnetization direction to an electrical potential difference using the huge magnetic-reluctance phenomenon of a ferromagnetic. Rewriting of the information in the ferromagnetic cel of such MRAM is performed by transforming the magnetization direction of a ferromagnetic cel by the magnetic field as for which induction was carried out to wiring for writing by a sink and its current in the current. About the structure and the actuation approach of the ferromagnetic cel, it is shown by R.E.Scheuerlein (1998 Proc.of Int NonVolatile Memory Conf.P47) and what allotted a total of every one pair of two pairs of crossing writing and read-out lines, and the thing which becomes one pair of wiring which served both as crossing writing and read-out line, a memory cell containing a huge magnetic-reluctance thin film, and this from the diode connected at the serial are proposed.
[0004] Moreover, there is also magnetic-thin-film memory which combined the memory cell containing one pair of wiring which served as crossing writing and read-out line which is indicated by JP,6-84347,A, the field effect transistor for cel selection, and a huge magnetic-reluctance thin film. The outline configuration of the memory cell of this magnetic-thin-film memory is shown in drawing 15 .
[0005] Reference of drawing 15 constitutes this magnetic-thin-film memory from a memory cell which consists of the magnetic-thin-film memory device 101 and the switching elements 102, such as FET, which were prepared at each intersection of the data line 103 by which two or more arrangement was carried out in the direction of a train, and the these sense lines 104 and the data line 103 so that it may cross with the sense line 104 by which two or more arrangement was carried out at the line writing direction, and these sense lines 104. The source (or drain) is connected with the data line 103, the gate is connected with a sense line 104, and, as for the switching element 102, the drain (or source) is connected with the end of the magnetic-thin-film memory device 101. The other end of the magnetic-thin-film memory device 101 is grounded. Resistance 106 is connected to the data line 103 at the serial.
[0006] By this magnetic-thin-film memory, when recording "1", the electrical potential difference of +3V is

first applied to the data line 103. Subsequently, if the electrical potential difference of +4V is applied to a sense line 104, a switching element 102 will be turned on and a comparatively big current will flow to the magnetic-thin-film memory device 101 and the data line 105. The data line 105 will be located directly under the magnetic-thin-film memory device 101, and that part will turn to it in the direction of predetermined in the sense of magnetization of the magnetic layer of the magnetic-thin-film memory device 101 by the field produced when a current flows to this data line 105.

[0007] On the other hand, when recording "0", the electrical potential difference of -3V is applied to the data line 103, and the electrical potential difference of -4V is applied to a sense line 104. Thereby, a switching element 102 is turned on and a comparatively big current (in record of the above "1", it is the current of the reverse sense) flows to the magnetic-thin-film memory device 101 and the data line 105. By the field produced when a current flows to this data line 105, the sense of magnetization of the magnetic layer of the magnetic-thin-film memory device 101 serves as a case of record of the above "1" with the reverse sense.

[0008] Information record of "1" to memory and "0" is performed using the magnetization condition of the above "1" and "0." It is specifically [both] the magnetization condition (in this case) of "0" about the magnetization condition of the 1st and 2nd magnetic layers of a magnetic-thin-film memory device. The case where considered the case where it was presupposed that the sense of magnetization of each magnetic layer turns into the same direction as information record of "0", and the magnetization condition of the 1st and 2nd magnetic layers is made into the magnetization condition (in this case, the sense of magnetization of each magnetic layer turns into reverse sense) of "1" and "0", respectively is considered as information record of "1."

[0009] In the above-mentioned information record, it uses that the resistance of a magnetic-thin-film memory device changes with sense of magnetization of each magnetic layer. Also in read-out of information, it uses that the resistance of a magnetic-thin-film memory device changes with sense of magnetization of each magnetic layer. That is, read-out of information is performed by detecting the electrical-potential-difference change according to the resistance of the magnetic-thin-film memory device to which information record was performed as mentioned above.

[0010] Recently, a magnetic memory device which was mentioned above is chip-ized, and the attempt used as program storing memory of a pocket mold information processor (the personal computer of a pocket mold, a portable telephone, etc. are included) is made.

[0011]

[Problem(s) to be Solved by the Invention] Although informational storage and playback are performed in the memory cell containing a huge magnetic-reluctance thin film by the direction of magnetization using the so-called magneto-resistive effect from which current resistance differs as mentioned above, generally the magnetic-reluctance rate of change is small. For example, if only 20 - 30% or less of resistance change is caused at the time of electrical-potential-difference impression of an about [0.3V] but applied voltage becomes large also in the case of the tunnel magnetic resistance element (Tunnel Magneto-Resistance;TMR) which shows a big magnetic-reluctance change, magnetic-reluctance rate of change will become small quickly. On the other hand, by the memory formed by the silicon semiconductor device production technique of high accumulation, an about [1-5V] electrical potential difference is impressed, and the voltage variation beyond about 0.1-0.2V is usually detected. When only a small electrical potential difference is applied to a memory cell, since the range of fluctuation of MRAM of magnetic reluctance is small, it is very difficult to MRAM to use a silicon semiconductor device production technique and to produce MRAM of high accumulation, so that this may show.

[0012] As what conquers this technical problem, the thing of a configuration (2T2R) of having combined two field effect transistors and two tunnel magnetic resistance elements (TMR) is proposed in one cel (2000 Proc.of Int Solid-State Circuits Conf.P128). The memory cell of this 2T2R structure is shown in drawing 16 .

[0013] A memory cell 200 consists of two TMR component R1a to which resistance is set complementary, R1b, and two field effect transistor TR1a and TR1b in drawing 16 . In case the gate of each field effect transistor TR1a and TR1b is connected to the read-out line RL1 and storage information is read, TMR component R1a is chosen by field effect transistor TR1a, and TMR component R1b is chosen by field effect transistor TR1b. The end of TMR component R1a is connected to sense line SL1a, the end of TMR component R1b is connected to sense line SL1b, and reading appearance of the storage information is carried out by comparing the potential between each sense line SL1a and SL1b. The writing (magnetization) of the information on TMR component

R1a is performed by passing a current to the write-in line WL1 and sense line SL1a, and the writing (magnetization) of the information on TMR component R1b is performed by passing a current to the write-in line WL1 and sense line SL1b.

[0014] In the case of the storage element which has the memory cell of the above-mentioned 2T2R structure, signal strength can be enlarged by setting up resistance of two TMR(s) complementary. However, since two field effect transistors are needed for one cel, as compared with the thing (configuration which combined one field effect transistor and one TMR for one cel) of 1T1R structure, it has the fault that cel area becomes large twice [about].

[0015] The thing of 1T1R structure given in JP,6-84347,A can change resistance to some extent by the case where it becomes the reverse sense to the case where it is possible to make cel area small and the sense of magnetization of each magnetic layer of magnetic-thin-film memory is this direction, mutually. However, when integrating to altitude, too, the range of fluctuation of magnetic reluctance is still small, and it is difficult to stabilize and detect storage information to a high speed and accuracy.

[0016] In the conventional ferromagnetic non-volatile storage element equipped with the memory cell containing a huge magnetic-reluctance thin film from the above actual condition, when integrating to altitude, it has the following problems.

[0017] In order to obtain sufficient signal strength, it is necessary to enlarge cel area, and it will become disadvantageous in respect of a miniaturization.

[0018] Furthermore, since the magnetic-reluctance rate of change at the time of impressing a detection electrical potential difference is small, it is difficult to stabilize and detect storage information to a high speed and accuracy.

[0019] It was still difficult to realize the component which can oppose DRAM (Dynamic Randum Access Memory) etc. with the conventional ferromagnetic storage element from the above problems. Moreover, although to use a ferromagnetic storage element as program storing memory of a pocket mold information processor was tried recently, memory which has the engine performance equivalent to the thing using DRAM was not realized until now, but implementation of such equipment was also set to one of the technical problems from the above problems.

[0020] While the object of this invention can solve the above-mentioned conventional technical problem and can make cel area small, magnetic-reluctance rate of change is to offer the ferromagnetic non-volatile storage element which can accumulate a small fence on the altitude which can detect storage information to a high speed and accuracy, and its information playback approach.

[0021] Other objects of this invention are to offer the memory chip and pocket mold information processor which have such a ferromagnetic non-volatile storage element.

[0022]

[Means for Solving the Problem] In order to attain the above-mentioned object, the ferromagnetic non-volatile storage element of this invention is characterized by the unit cell which constitutes 1-bit memory consisting of the 1st and 2nd magnetic resistance elements magnetized so that the sense of mutual magnetization may turn into reverse sense, and one solid state switch component for choosing these 1st and 2nd magnetic resistance elements.

[0023] In the above-mentioned case, said solid state switch component is connected common [a drain terminal] to one [each] terminal of said 1st and 2nd magnetic resistance elements. A source terminal is grounded, and it is constituted so that these drain terminal and a source terminal may be electrically connected by a predetermined electrical potential difference being impressed to a gate terminal. You may constitute so that the other-end child of said 1st and 2nd magnetic resistance element may have further the 1st and 2nd bit line connected, respectively and the sense amplifier which compares the electrical-potential-difference value according to the magnetization condition of said 1st and 2nd magnetic resistance elements produced in said 1st and 2nd bit lines.

[0024] Moreover, you may constitute so that one terminal of said 1st and 2nd magnetic resistance element may be connected to the drain terminal of said solid state switch component through diode, respectively.

[0025] Furthermore, said 1st and 2nd magnetic resistance element is equipped with the 1st [which has an easy axis], and 2nd ferromagnetic film in the predetermined direction, respectively. Said a part of 1st bit line is located in right above [of said 1st ferromagnetic film]. Said a part of 2nd bit line is located in right above [of

said 2nd ferromagnetic film]. It has further write-in wiring which passes directly under said 1st and 2nd ferromagnetic film. While said 1st ferromagnetic film is magnetized in the predetermined direction in accordance with an easy axis by the magnetic field which produces the current of predetermined magnitude by passing in the predetermined direction to the both sides of said 1st bit line and write-in wiring You may constitute so that said 2nd ferromagnetic film may be magnetized in the predetermined direction in accordance with an easy axis by the magnetic field which produces the current of predetermined magnitude by passing in the predetermined direction to the both sides of said 2nd bit line and write-in wiring.

[0026] The 1st and 2nd magnetic resistance element by which the information playback approach of this invention was connected to the 1st and 2nd bit line with which a predetermined electrical potential difference is supplied, respectively and by which the sense of mutual magnetization is magnetized so that it may become the reverse sense, It is the information playback approach of a ferromagnetic non-volatile storage element that the unit cell which constitutes 1-bit memory from one solid state switch component for choosing these 1st and 2nd magnetic resistance elements is constituted. The 1st electrical-potential-difference value of said 1st bit line which chooses said 1st and 2nd magnetic resistance elements by making said solid state switch component into an ON state, and is produced according to the magnetic-reluctance value of the 1st this chosen magnetic resistance element, the 2nd electrical-potential-difference value of said 2nd bit line produced according to the magnetic-reluctance value of the 2nd this selected magnetic resistance element -- comparing -- electrical-potential-difference value [of ** a 1st] > -- the case of the 2nd electrical-potential-difference value -- the 1st information -- carrying out -- the 1st electrical-potential-difference value -- < -- it is characterized by reading the case of the 2nd electrical-potential-difference value as the 2nd information.

[0027] The memory chip of this invention is characterized by forming one of above-mentioned ferromagnetic non-volatile storage elements on a semi-conductor substrate.

[0028] The pocket mold information processor of this invention is characterized by having the program storing memory which consists of one of above-mentioned ferromagnetic non-volatile storage elements, and the control means which operates according to the program stored in this program storing memory.

[0029] According to this invention as above-mentioned, since a unit cell (memory cell) is constituted by two magnetic resistance elements and one solid state switch, the cel area becomes smaller than the thing of 2T2R structure.

[0030] Moreover, according to this invention, the problem accompanying the magnetic-reluctance rate of change at the time of impressing the detection electrical potential difference mentioned above according to the following operations being small is solvable.

[0031] a magnetic resistance element -- the sense of magnetization -- the electric resistance values differ. In the ferromagnetic non-volatile storage element of this invention, it consists of the 1st and 2nd magnetic resistance elements magnetized so that the sense of the magnetization with a mutual unit cell (memory cell) may turn into reverse sense, and storage of 1-bit information is performed according to the combination of the sense of magnetization of these 1st and 2nd magnetic resistance elements. That is, it is remembered complementary that the size relation of the resistance of the 1st and 2nd magnetic resistance elements conflicts. For example, the size relation of the resistance of the 1st and 2nd magnetic resistance elements sets the case of the "0" and 1st magnetic-resistance-element > 2nd magnetic resistance element to "1" for the case of the 1st magnetic-resistance-element < 2nd magnetic resistance element, and information is memorized.

[0032] When 1-bit storage is memorized as mentioned above due to the size resistance of the 1st and 2nd magnetic resistance elements, playback (read-out) of the storage information is performed based on the size relation of the resistance of each magnetic resistance element. That is, any of the resistance of the 1st magnetic resistance element and the resistance of the 2nd magnetic resistance element are small, or (or is it large either?) reading appearance of the information is carried out. Informational playback is performed by comparing the electrical-potential-difference value according to the size relation of the above-mentioned resistance which the 1st and 2nd magnetic resistance element specifically produces in the 1st and 2nd bit line connected, respectively. Thus, if it is made for the electrical potential difference generated in each bit line to turn into reference voltage mutually, it becomes unnecessary to count upon voltage variation, such as a part for the temperature characteristic, and a wire length, and can operate also with small magnetic-reluctance rate of change.

[0033] Furthermore, since according to this invention selection of a memory cell is performed by one solid state

switch and it is not necessary to expect dispersion in a selection transistor in comparison with the thing of the cellular structure of the conventional 2T2R, it can operate with still smaller magnetic-reluctance rate of change.
[0034] Furthermore, among this inventions, since the direction where a current flows with diode in that by which one terminal of the 1st and 2nd magnetic resistance element is connected to the drain terminal of a solid state switch component through diode, respectively is restricted, the penetration current which flows to one magnetic resistance element does not flow to the magnetic-resistance-element side of another side.
[0035]
[Embodiment of the Invention] Next, the operation gestalt of this invention is explained with reference to a drawing.
[0036] (Operation gestalt 1) The fragmentary sectional view of the memory cell of the ferromagnetic non-volatile storage element which shows the circuit diagram in which drawing 1 shows the configuration of the ferromagnetic non-volatile storage element of the 1st operation gestalt of this invention, and drawing 2 to drawing 1 , and drawing 3 are the partial perspective views of the memory cell of the ferromagnetic non-volatile storage element shown in drawing 1 . Hereafter, with reference to drawing 1 -3, the configuration of the ferromagnetic non-volatile storage element of this gestalt is explained to a detail.
[0037] When drawing 1 is referred to, the ferromagnetic non-volatile storage element of this gestalt the bit line ("BL1a and BL1b", and "BL2a and BL2b" --) of the couple of plurality [line writing direction] "BL3a and BL3b" are arranged, and two or more word line (WL1, WL2, WL3) and two or more write-in lines (L1, L2, L3) are arranged in the direction of a train so that these bit lines may be intersected. The memory cell which constitutes the 1-bit memory which consists of a variable resistor of the couple which can choose an electric resistance value as each intersection of a bit line and a word line by choosing the magnetization direction of one field effect transistor and ferromagnetic is arranged (matrix array). In the example shown in drawing 1 , so that the address in a matrix array can be specified The sign of "T11, T12, T13, T21, T22, T23, T31, T32, T33" is given to the field effect transistor. To the variable resistor of a couple The sign of "R11a, R12a, R13a, R21a, R22a, R23a, R31a, R32a, R33a", and "R11b, R12b, R13b, R21b, R22b, R23b, R31b, R32b, R33b" is attached, respectively.
[0038] The transistor for address selections is prepared in each end of the line by which a pair each of bit lines ("BL1a and BL1b", "BL2a and BL2b", "BL3a and BL3b") serve as a pair, respectively, and the other end is connected to the sense amplifier. As for each write-in lines L1, L2, and L3, the transistor for the change of the sense of address selection and a current is prepared in ends, respectively.
[0039] A sense amplifier operates as a comparator (comparator), there are "+ terminal" and a "- terminal" in the input terminal, and the bit line of a couple is connected to both [these] input terminals. the electrical-potential-difference comparison actuation in this sense amplifier -- "+ terminal voltage" > "- terminal voltage"
the time of ** -- yes -- output (namely, Vdd) and "+ terminal voltage" < "- terminal voltage"
It becomes a low output (namely, 0V) at the time of **.
[0040] The configuration of each memory cell is the same. Here, the configuration is concretely explained about the memory cell enclosed with the broken line of the center section of drawing 1 . This memory cell consists of one field effect transistor T22, and variable-resistor R22a of a couple and R22b. the gate is connected with a word line WL2, and the source grounds a field effect transistor T22 -- having -- a drain -- each -- it connects common to the end of variable-resistor R22a and R22b. The other end of variable-resistor R22a is connected with bit line BL2a, and the other end of variable-resistor R22b is connected with bit line BL2b. It is drawing 2 and drawing 3 which showed the outline structure of this memory cell typically. Hereafter, with reference to drawing 2 and drawing 3 , memory cell structure is further explained to a detail.
[0041] On the semi-conductor substrate 1, a well-known high accumulation silicon semiconductor device production technique is used, the source 2, a drain 3, and gate dielectric film 4 are formed, and the gate electrode 5 which consists of a conductor is further formed on gate dielectric film 4. This part is equivalent to the field effect transistor T22 shown in drawing 1 . In this field effect transistor, by impressing a predetermined electrical potential difference to the gate electrode 5, and controlling the carrier consistency of the field (between the source 2 and drains 3) of gate electrode 5 directly under, the current which flows between the source 2 and a drain 3 is controlled, and magnification actuation or ON, and off actuation are performed. The source 2 is electrically connected with a grounding conductor 8 through the source contact plug 7, and the drain 3 is electrically connected with the local wiring 10 through the drain contact plug 6.

[0042] On the grounding conductor 8, it writes in so that this grounding conductor 8 may be met, and wiring 9 (it is equivalent to the write-in line L2 of drawing 1) is formed. It writes in with this grounding conductor 8, and wiring 9 is insulated. Some write-in wiring 9 has lapped with some above-mentioned local wiring 10, and it insulates between both wiring. In the lap parts of this write-in wiring 9 and the local wiring 10, the local wiring 10 is written in, it is located on wiring 9, and the variable resistors (magnetic resistance element) 13 and 14 (it is equivalent to variable-resistor R22a [of drawing 1] and R22b, respectively.) of a couple are formed on this local wiring 10. The upper part is in contact with the bit line 15 (it is equivalent to bit line BL2a of drawing 1 .), and the variable resistor 13 is in contact with the terminal 11 by which the lower part was electrically connected with the local wiring 10. Similarly, the upper part is in contact with the bit line 16 (it is equivalent to bit line BL2b of drawing 1 .), and the variable resistor 14 is in contact with the terminal 12 by which the lower part was electrically connected with the local wiring 10. Here, variable resistors 13 and 14 are variable resistors which can choose an electric resistance value by choosing the magnetization direction of a ferromagnetic, for example, a ferromagnetic ingredient with a big magneto-resistive effect like GMR or a CMR ingredient is used, and the resistance over the current which flows a ferromagnetic changes depending on the sense of the magnetization, or the existence of magnetization. Thus, in the constituted variable resistors 13 and 14, resistance can be chosen by choosing the magnetization direction of a ferromagnetic by the external magnetic field. Although GMR and a CMR ingredient are used, the TMR component which used the tunnel insulator layer for others is one of those can expect the same actuation.

[0043] Here, a TMR component is explained briefly. TMR has the structure which sandwiched the tunnel insulator layer by the software layer (ferromagnetic layer with small coercive force), and the hard layer (ferromagnetic layer with large coercive force), it is with the case where the magnetization direction of both layers is parallel, and the case where it is the reverse sense, and the resistance when passing a penetration current differs. Nonvolatile memory is realized using this property. When using a TMR component, rewriting of the memorized information has two kinds, the case where only the magnetization direction of a software layer is rewritten, and when the magnetization direction of both the layers of a software layer and a hard layer is rewritten, and can be suitably chosen according to a design.

[0044] Next, the writing and read-out actuation of the information in the ferromagnetic non-volatile storage element shown in drawing 1 are explained. it can set to each memory cell -- writing and reading appearance are carried out, and since actuation is the same, it can be set by the following explanation to the memory cell (memory cell surrounded with the broken line of the center of drawing 1) of a center section -- writing and reading appearance are carried out, and actuation is mentioned as an example and explained.

[0045] (1) Read-out actuation : here, the reverse sense is always magnetized and explain variable-resistor R22a of a couple, and R22b as what the resistance is also remembered that size relation conflicts complementary.

[0046] First, supply voltage Vdd is impressed to the left end of each bit line BL2a and BL2b, respectively, a predetermined electrical potential difference is impressed to a word line WL2, and a transistor T22 is made into an ON state. if a transistor T22 is turned on -- each -- the stationary current flows to variable-resistor R22a and R22b. this time -- each -- since the magnetization direction is remembered that it has reverse sense mutually and size relation conflicts also in that resistance as above-mentioned, an electrical-potential-difference difference produces variable-resistor R22a and R22b between the input terminals of the sense amplifier to which each bit line BL2a and BL2b are connected (redistribution of a charge arise between the capacity and the variable resistors which a bit line has). By this, either "Vdd" or "0V" will be chosen [which of variable-resistor R22a and R22b] for the output of a sense amplifier by whether it is high resistance.

[0047] Usually, although a dozens of mV electrical-potential-difference difference is detected and a sense amplifier can operate it, since it was necessary to generate the electrical-potential-difference difference exceeding a part for dispersion of the on resistance of a bit line edge and the transistor for selection, or the resistance of a variable resistor, it needed to take the very large magnetic-reluctance rate of change of a variable resistor conventionally. In the ferromagnetic non-volatile storage element of this operation gestalt, since two variable resistors which constitute a memory cell approach extremely and are arranged, dispersion in resistance is dramatically small.

[0048] Moreover, in the ferromagnetic non-volatile storage element of this operation gestalt, the variable resistor of the couple which constitutes a memory cell operates complementary, and, as for the electrical potential difference generated on each line of one pair of bit lines, each becomes reference voltage. Thus, if it is

made for the electrical potential difference generated in each bit line to turn into reference voltage mutually, it becomes unnecessary to count upon voltage variation, such as a part for the temperature characteristic, and a wire length, and can operate also with small magnetic-reluctance rate of change.
[0049] Furthermore, in the ferromagnetic non-volatile storage element of this operation gestalt, since it is not necessary to expect dispersion in a selection transistor in comparison with the cellular structure of 2T2R, it can operate with still smaller magnetic-reluctance rate of change.
[0050] (2) Write-in actuation : here, explain the actuation which writes desired magnetization only in two software layers, variable-resistor R22a and R22b (variable resistors 13 and 14 of drawing 3 R> 3), which constitute a memory cell. Here, the reverse sense is always magnetized and variable-resistor R22a and R22b are explained as what the resistance is also remembered that size relation conflicts complementary.
[0051] First, in order to write magnetization in variable-resistor R22a, it writes in with bit line BL2a (bit line 15 of drawing 3), and the current of the predetermined sense is passed on a line L2 (write-in wiring 9 of drawing 3). Drawing 4 is the mimetic diagram showing the sense of the current at this time, and the sense of a field. Drawing 5 is drawing showing the situation of the flux reversal of the memory cell at the time of the writing shown in drawing 4 , and the mimetic diagram showing the condition of magnetization when the mimetic diagram showing the condition of the magnetization when (a) writing in and passing a current to wiring at the predetermined sense and (b) pass a current to the predetermined sense at a bit line, and (c) are the mimetic diagrams which looked at the magnetic-reluctance machine of the condition of (b) from the top. The cellular structure shown in drawing 4 and 5 is the same as what was shown in drawing 3 , and attaches the same sign. Hereafter, with reference to drawing 4 and 5, the flux reversal of the memory cell at the time of writing is explained.
[0052] Although it writes in the write-in wiring 9, it will write in if a current I2 flows, and a magnetic field H2 occurs, as shown in drawing 5 (a), the magnetization direction of a variable resistor (magnetic resistance element) 13 is not reversed only in this write-in magnetic field H2. Here, the magnetization direction of a variable resistor 13 shall have turned to the direction of reverse beforehand with the direction of the magnetic field component of the write-in magnetic field H2. Moreover, the shaft (easy axis) which is easy to be magnetized writes in variable-resistor R22a, and it has become in parallel with the direction of the magnetic field component of a magnetic field H2 (it is parallel to a bit line 15).
[0053] When it writes in a bit line 15 in the condition that the above-mentioned write-in magnetic field H2 is impressed and a current I1 flows, the write-in magnetic field H1 will occur, and both the magnetic fields of this write-in magnetic field H1 and the above-mentioned write-in magnetic field H2 will be impressed to a variable resistor 13. Here, the magnetic field component of the write-in magnetic field H1 is generated in the direction which becomes vertical to the magnetic field component of the write-in magnetic field H2. Thus, magnetization of a variable resistor 13 is reversed for the first time by writing in and both the magnetic fields of magnetic fields H1 and H2 being impressed simultaneously (refer to drawing 5 (b) and drawing 5 (c)).
[0054] As mentioned above, with this gestalt, only by passing a current to the write-in wiring 9 or a bit line 15, it is not reversed, and the magnetization direction of a variable resistor 13 is passing a current simultaneously on both lines, and the magnetization direction of a variable resistor 13 reverses it for the first time. Thereby, flux reversal of the desired variable resistor can be selectively carried out [from] among the variable resistors arranged in the shape of a matrix.
[0055] If the writing of magnetization of variable-resistor R22a is performed as mentioned above, the writing of magnetization of variable-resistor R22b will be performed. When writing magnetization in variable-resistor R22b, it writes in with bit line BL2b (bit line 16 of drawing 3), and, in the above-mentioned variable-resistor R22a, the current of hard flow is passed on a line L2 (write-in wiring 9 of drawing 3). Also in this case, reversal of magnetization arises for the first time like the case of the above-mentioned variable-resistor R22a by writing in with a bit line 16 and passing a current to the both line of wiring 9.
[0056] the condition of it having been magnetized with this gestalt in the direction which showed variable-resistor R22a to drawing 5 (a), for example, and having magnetized variable-resistor R22b towards the reverse -- "0 -- " -- then -- each -- the information on "1" can be written in by reversing magnetization of variable-resistor R22a and R22b by above-mentioned write-in actuation.
[0057] It can write in and read-out actuation can attain the working speed which was explained above and which is equal to DRAM. Moreover, cel area in this case can be made into a thing smaller than MRAM with

2T2R structure.
[0058] Next, a configuration is explained to a detail with the making process about the example of the ferromagnetic non-volatile storage element of this operation gestalt.
[0059] (Example) Drawing 6 (a) - (g) is the process sectional view showing the production procedure of the memory cell of the ferromagnetic non-volatile storage element shown in drawing 2 and drawing 3 . According to this example, first, as shown in drawing 6 (a), the source 2, a drain 3, gate dielectric film 4, and the gate electrode 5 are formed on the semi-conductor substrate 1, and the substrate containing MOS(Metal-Oxide-Semiconductor)-FET (Field Effect Transistor; field effect transistor) is produced. Contact holes 7a and 6a are opened in the source 2 of FET in this substrate, and the part of a drain 3, respectively, and a plug is embedded into them (refer to drawing 6 (b)). Ti barrier film is used for a substrate.
[0060] Subsequently, as a wiring layer, after forming a Ti/AlSiCu/Ti layer, it is processed into a predetermined pattern according to a well-known FOTORISO process, a part for a grounding conductor 8 and a plug connection is formed, SiO2 film 20 by the well-known plasma-CVD method is further formed as an interlayer insulation film, and flattening of the top face is carried out (refer to drawing 6 (c)).
[0061] Subsequently, as a wiring layer, after forming a Ti/AlSiCu/Ti layer, it is processed into a predetermined pattern according to a FOTORISO process, the write-in wiring 9 is formed, SiO2 film 21 by the well-known plasma-CVD method is further formed as an interlayer insulation film, and flattening of the top face is carried out (refer to drawing 6 (d)).
[0062] Subsequently, W (tungsten) layer as a path cord to a TMR component is formed, it is processed into a predetermined pattern according to a FOTORISO process, and the local wiring 10 is formed (refer to drawing 6 (e)). Subsequently, after forming a NiFe/AlOx/Co cascade screen as AlCu layer and TMR component 13a as a substrate layer used as a terminal 11 and processing a predetermined configuration according to a FOTORISO process, SiO2 film 22 is formed by the plasma-CVD method, and flattening of the top face is carried out (refer to drawing 6 (f)).
[0063] Subsequently, after forming the Ti/AlSiCu/Ti layer used as the bit line 15 which served as the writing ray, it is processed into a predetermined pattern according to a FOTORISO process, and SiO2 film as an interlayer insulation film is formed by the plasma-CVD method, the SiN film 23 as a protective layer is formed further, a pad field is processed, and it is completed (refer to drawing 6 (g)).
[0064] The arrangement which looked at the memory cell produced with the predetermined design rule by the above making process from the top face is shown in drawing 7 , and arrangement of the memory cell of the conventional 2T2R structure designed by the same design rule for the comparison of cel area is shown in drawing 8 . the memory cell (drawing 8) of the conventional 2T2R structure -- cel area -- per [48 / about] bit -- the memory cell shown in drawing 7 to being F2 (F being the minimum processing dimension) -- cel area -- about 36 -- it was set to F2 and became about 25% of area reduction.
[0065] (Operation gestalt 2) The circuit diagram in which drawing 9 shows the configuration of the memory cell of the ferromagnetic non-volatile storage element of the 2nd operation gestalt of this invention, and drawing 10 are the partial perspective views showing the structure of the memory cell shown in drawing 9 . In the example shown in drawing 9 , for convenience, although only one memory cell is shown, also in this gestalt, the matrix array of the memory cell is carried out like the case of the 1st above-mentioned operation gestalt.
[0066] If drawing 9 is referred to, bit line BL1a of a couple and BL1b are arranged at a line writing direction, a word line WL1 and the write-in line L1 are arranged in the direction of a train so that these bit lines may be intersected, and the memory cell is formed in the intersection of these bit lines and a word line. This memory cell consists of two variable-resistor R1a which can choose an electric resistance value, R1b, and two diode D1a and D1b by choosing the magnetization direction of one field effect transistor TR and ferromagnetic. Bit line BL1a of a couple and BL1b are connected to "+ terminal" of the input terminal of a sense amplifier, and "- terminal", respectively.
[0067] The gate is connected with a word line WL1, the source is grounded and, as for the field effect transistor TR, the drain is connected to the end of each diode D1a and D1b in common. The other end of diode D1a and D1b is connected to the end of variable-resistor R1a and R1b, respectively. The other end of variable-resistor R1a is connected with bit line BL1a, and the other end of variable-resistor R1b is connected with bit line BL1b. It is drawing 10 which showed the structure of this memory cell typically.
[0068] The cellular structure shown in drawing 10 is almost the same as the cellular structure shown in drawing

3 except the PN-junction sections 40a and 40b being formed in a drain (P type) 3, variable resistors (magnetic resistance element) 13 and 14 being connected to the local wiring 10a and 10b, respectively, and the local wiring 10a and 10b being electrically connected to the PN-junction sections 40a and 40b through the drain contact plugs 6a and 6b. what was shown in drawing 3 among drawing 10 -- the same sign is given to the same configuration section.

[0069] If drawing 10 is referred to, on the semi-conductor substrate (N type) 1, a well-known high accumulation silicon semiconductor device production technique is used, the source (P type) 2, a drain (P type) 3, and gate dielectric film 4 are formed, and the gate electrode 5 which consists of a conductor is further formed on gate dielectric film 4. This part is equivalent to the field effect transistor TR shown in drawing 9 . The drain contact plugs 6a and 6b are formed in N fields each of the PN-junction sections 40a and 40b of a drain 3, respectively. These PN-junction sections 40a and 40b are equivalent to diode D1a shown in drawing 9 , respectively, and D1b.

[0070] Also in the ferromagnetic non-volatile storage element of this operation gestalt, although informational writing and read-out are performed by the same principle as the case of the 1st above-mentioned operation gestalt, by having arranged diode D1a and D1b, the sneak current between the following cels (between variable-resistor R1a and R1b) becomes small, and can realize more stable actuation.

[0071] Drawing 11 shows typically the sneak current between the cels at the time of read-out. When it does not have diode D1a and D1 which were shown in drawing 9 , sneak current as shown in drawing 11 depending on conditions arises. By the case where informational writing is specifically performed so that the resistance of b variable-resistor R1a may become lower than that of variable-resistor R1b, when the resistance of variable-resistor R1a is lower than the on resistance value of Transistor TR, the current which flows variable-resistor R1b flows to the variable-resistor R1a side (sneak current I1). By the case where similarly informational writing is performed so that the resistance of variable-resistor R1b may become lower than that of variable-resistor R1a, when the resistance of variable-resistor R1b is lower than the on resistance value of Transistor TR, the current which flows variable-resistor R1a flows to the variable-resistor R1b side (sneak current I2). In the example shown in drawing 9 R> 9, these sneak current I1 and I2 is inhibited by diode D1a and D1b. In this case, compared with the case of the 1st operation gestalt, about 4 figures of sneak current become small.

[0072] It is producible with the making process which also showed the ferromagnetic non-volatile storage element of this operation gestalt to above-mentioned drawing 6 (a) - (g). Cel area is almost the same as the thing of the 1st operation gestalt.

[0073] A TMR component can be used for a variable resistor (magnetic resistance element) in the ferromagnetic non-volatile storage element of the 1st [which was explained above] and 2nd operation gestalten. In that case, the sense of magnetization of the ferromagnetic film which constitutes a TMR component is usually made horizontal to membranous field inboard.

[0074] Drawing 12 is drawing showing the TMR component by which the ferromagnetic film is magnetized horizontally, and the mimetic diagram in which (a) shows the sense of the magnetization in the case of resistance size, and (b) are the mimetic diagrams showing the sense of the magnetization in the case of resistance smallness. This TMR component has the structure which sandwiched the tunnel insulator layer 40 by the ferromagnetic film 41 and 42, and resistance changes by controlling by the write-in actuation which mentioned above the sense of magnetization of the ferromagnetic film 41, and same actuation (flux reversal). When the magnetization direction of each ferromagnetic film 41 and 42 is this direction as are shown in drawing 12 (a), and the resistance of a TMR component becomes large and it is shown in drawing 12 (b), when the magnetization direction of each ferromagnetic film 41 and 42 is the reverse sense, specifically, the resistance of a TMR component becomes small. In addition, the ferromagnetic film 42 shall always be magnetized in the fixed direction. Moreover, the easy axis of each ferromagnetic film 41 and 42 is horizontal to film surface inboard.

[0075] As mentioned above, if cell size becomes small when magnetizing a TMR component horizontally, it turns out that the phenomenon which the magnetization direction reverses near a wall surface (near the boundary of the tunnel insulator layer 40 and the ferromagnetic film 41 and 42) and which is called curling occurs, and it becomes difficult to maintain magnetization to stability.

[0076] The ferromagnetic film which constitutes a TMR component can solve the problem of the above-mentioned curling phenomenon with constituting so that it may be perpendicularly magnetized to membranous

field inboard. Drawing 13 is drawing showing the TMR component with which the ferromagnetic film is magnetized perpendicularly, and the mimetic diagram in which (a) shows the sense of the magnetization in the case of resistance size, and (b) are the mimetic diagrams showing the sense of the magnetization in the case of resistance smallness. This TMR component has the structure which sandwiched the tunnel insulator layer 50 by the ferromagnetic film 51 and 52 which consists of Gd, Tb, etc., and resistance changes by controlling by the write-in actuation which mentioned above the sense of magnetization of the ferromagnetic film 51, and same actuation (flux reversal). When the magnetization direction of each ferromagnetic film 51 and 52 is this direction as are shown in drawing 13 (a), and the resistance of a TMR component becomes large and it is shown in drawing 13 (b), when the magnetization direction of each ferromagnetic film 51 and 52 is the reverse sense, specifically, the resistance of a TMR component becomes small. In addition, the ferromagnetic film 52 shall always be magnetized in the fixed direction. Moreover, the easy axis of each ferromagnetic film 51 and 52 has become perpendicularly to film surface inboard.

[0077] If it writes in with the bit line which served as the write-in line in the ferromagnetic non-volatile storage element of this operation gestalt carried out above and the ingredient which makes copper a subject constitutes a line, it will be lost that the dependability of the current which flows at the time of writing is spoiled, and it will become possible to operate the storage element of this gestalt to rear-spring-supporter stability at a long period of time. Generally, if the current of big current density is passed to wiring, it is known that the phenomenon called "electromigration" will occur. The conduction electron style in a metal washes away a metal atom gradually, a this "electromigration" phenomenon is made to transform wiring, and, finally a short circuit and an open circuit are caused. It can write in with the bit line which served as the write-in line, and the short circuit by such "electromigration" phenomenon and an open circuit can be inhibited with constituting a line with the ingredient which makes copper a subject.

[0078] Furthermore, by using SiGe for the channel part of the field effect transistor which constitutes a memory cell, or applying a SOI (Silicon On Insulator) technique to production of a substrate, from the thing of the usual metal-oxide-semiconductor structure, a high speed can be operated and the access time of a storage element etc. can be shortened. Here, a SOI technique is forming thin Si film on an insulator layer, and building an MOS IC in the Si film, and it says forming a three-dimension integrated circuit. According to this SOI technique, the substrate and parasitic capacitance used as the hindrance of improvement in the speed of an MOS transistor can be reduced.

[0079] It is possible to offer the memory function by which the power source was stabilized also on the unstable service condition taking advantage of the so-called non-volatile function in which information is not lost even if it intercepts a power source by using the ferromagnetic non-volatile storage element of this operation gestalt in pocket mold information processors, such as a memory chip, and pocket type communication equipment, a personal computer machine. Moreover, when backing up the conventional SRAM (Static Random Access Memory) by the cell and using it as work-piece memory, if the storage element of this gestalt is used, it becomes unnecessary and a backup power supply can contribute to the cutback of cost, and the miniaturization of equipment greatly. The processing engine performance of pocket mold information processors, such as pocket type communication equipment and a pocket type personal computer, can be raised by leaps and bounds further again instead of the NOR mold flash memory which was being used as program memory by using the storage element of this gestalt rewritable at several figures high speed.

[0080] Hereafter, the memory chip and pocket mold information processor using the ferromagnetic non-volatile storage element of this invention are explained.

[0081] (1) Memory chip : the ferromagnetic non-volatile storage element (memory array) was formed on the semi-conductor substrate with the making process shown in drawing 6 (a) - (g), and the memory chip was produced. After adding the actuation circuit compatible with EEPROM (Electrical Erasable and Programmable ROM), this memory chip was carried in the leadframe (it consists of the outer lead section for soldering to the chip loading section, the inner lead section of wire bonding, and a substrate with metal goods with single frame structure.), and was enclosed with the ceramic package. Thus, as for the produced memory device, after the stress of 1 hour operated normally at 40 degrees C.

[0082] Moreover, it is also possible to arrange the control circuit (for a 8-bit microprocessor etc. to be included) which performs writing of the information in the above-mentioned ferromagnetic non-volatile storage element and this ferromagnetic non-volatile storage element and control of read-out, and various circuits, and to,

constitute an embedded-type MAG memory chip in addition to this, on the same chip.
[0083] (2) Pocket mold information processor : this pocket mold information processor is equipped with the nonvolatile memory which consists of a ferromagnetic non-volatile storage element of the above-mentioned 1st and the 2nd operation gestalt as program storing memory, and it constitutes it so that it may operate according to the program in which the control circuit was stored in the program storing memory. As an example, the outline configuration of the pocket mold information processor which has communication facility in drawing 14 is shown.
[0084] In drawing 14 , a pocket mold information processor has the program storing memory 60 in which the predetermined program was stored, the control section 61 which operates according to the program stored in the program storing memory 60, the communications department 62 which can transmit and receive the information through wire circuits (common public networks, such as the telephone line, ISDN, etc.) or a wireless circuit, the displays 63, such as a liquid crystal display, the storage section 64, and the input sections 65, such as a keyboard. A control section 61 exchanges information on the information terminal of the exterior through the communications department 62, or displays information on a display 63. Moreover, a control section 61 can also make the result of an operation memorize to the storage section 64. In addition, a control section 61 can perform various processings and control according to the input from the input section 65. The operation by such control section 61 and control have realized the thing near the function of the existing personal computer.
[0085] As mentioned above, this pocket mold information processor can realize the almost same engine performance as the case where DRAM is used, using a ferromagnetic non-volatile storage element as program storing memory.
[0086] In addition, although constituted from this pocket mold information processor by the 1st or 2nd ferromagnetic non-volatile storage element which the program storing memory 60 mentioned above, it is also possible the storage section 64 and to constitute from the ferromagnetic non-volatile storage element similarly.
[0087]
[Effect of the Invention] As explained above, according to this invention, the component structure and the actuation approach of detecting storage information at a high speed as magnetic-reluctance rate of change is small can be offered. For this reason, stability can be provided with the non-volatile MAG memory in which R/W actuation is possible using small applied voltage.
[0088] Moreover, since it is the memory cell of 1T2R structure, compared with the thing of the cellular structure of 2T2R, non-volatile MAG memory with a small cel area can be offered.

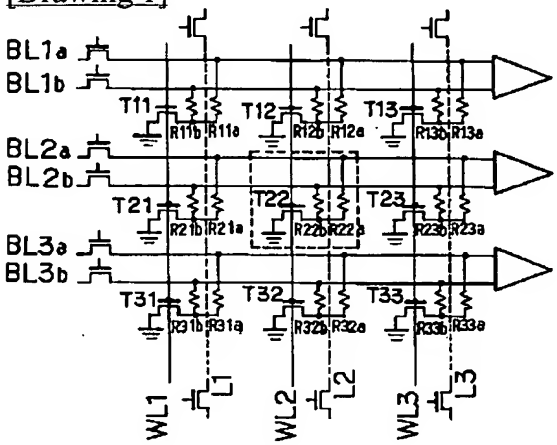
[Translation done.]

* NOTICES *

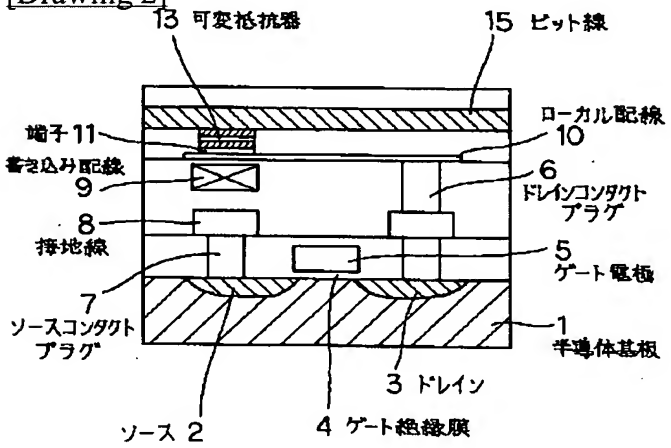
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

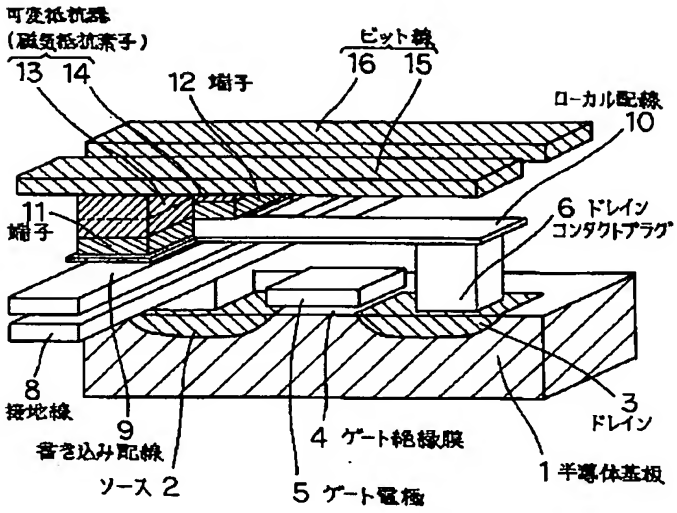
[Drawing 1]



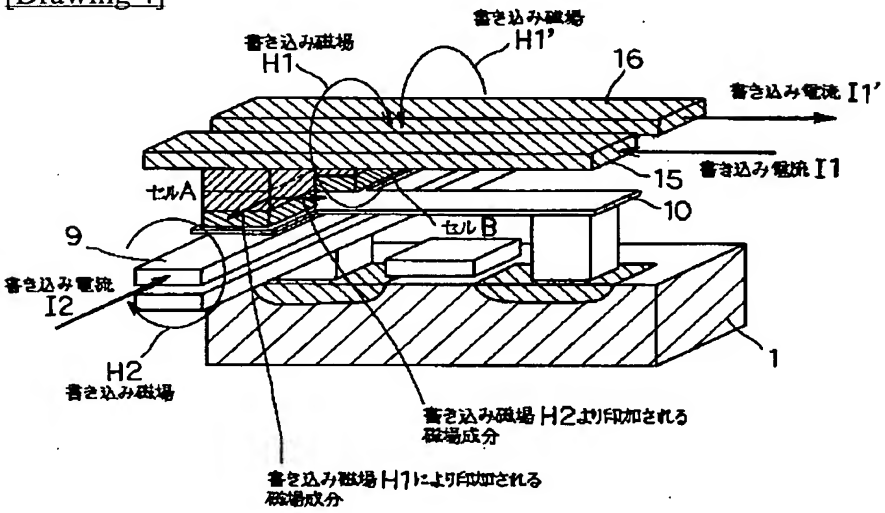
[Drawing 2]



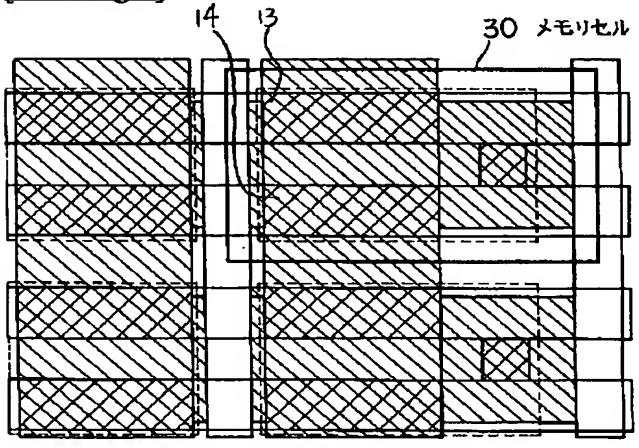
[Drawing 3]



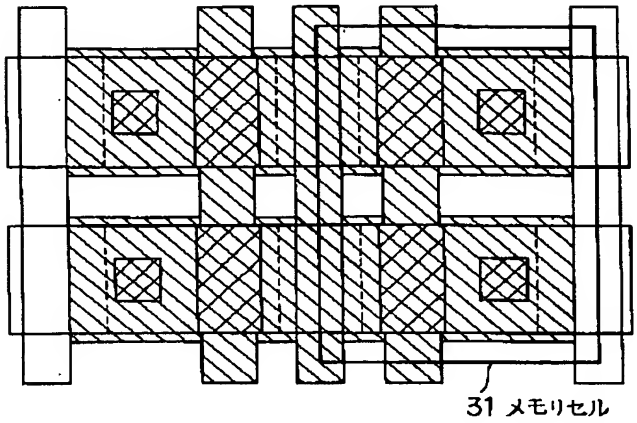
[Drawing 4]



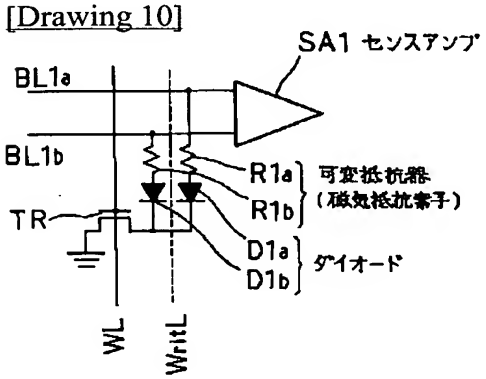
[Drawing 7]



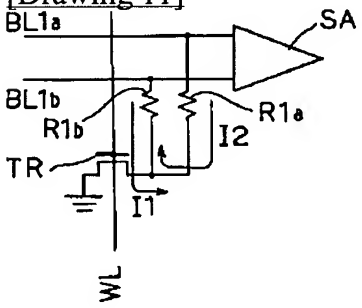
[Drawing 8]



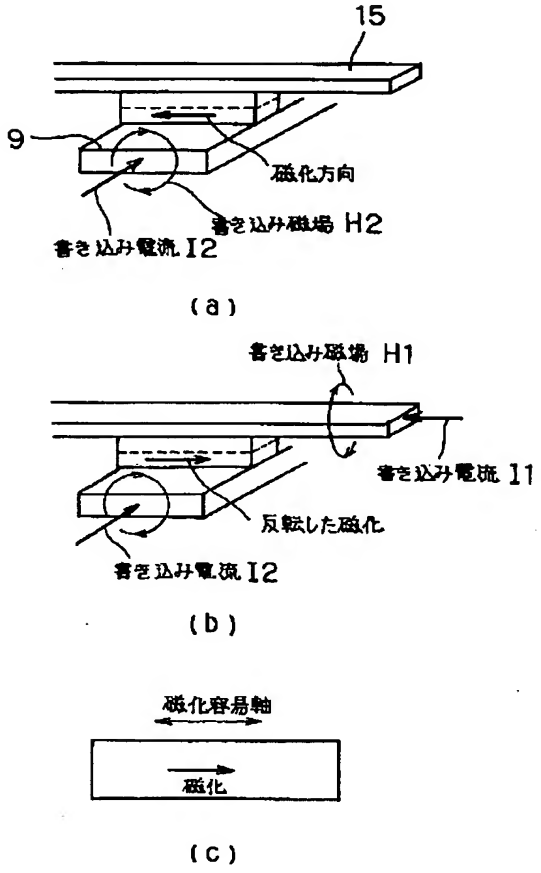
[Drawing 10]



[Drawing 11]



[Drawing 5]



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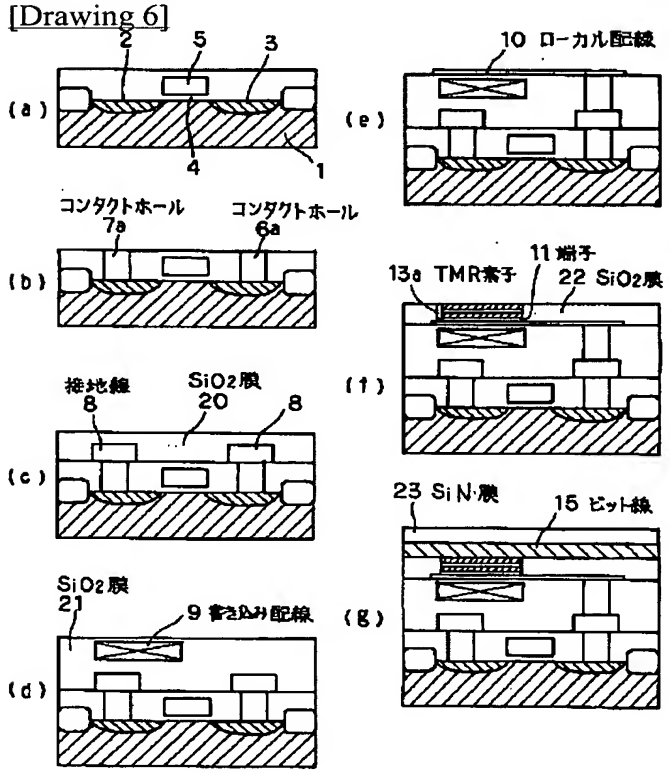
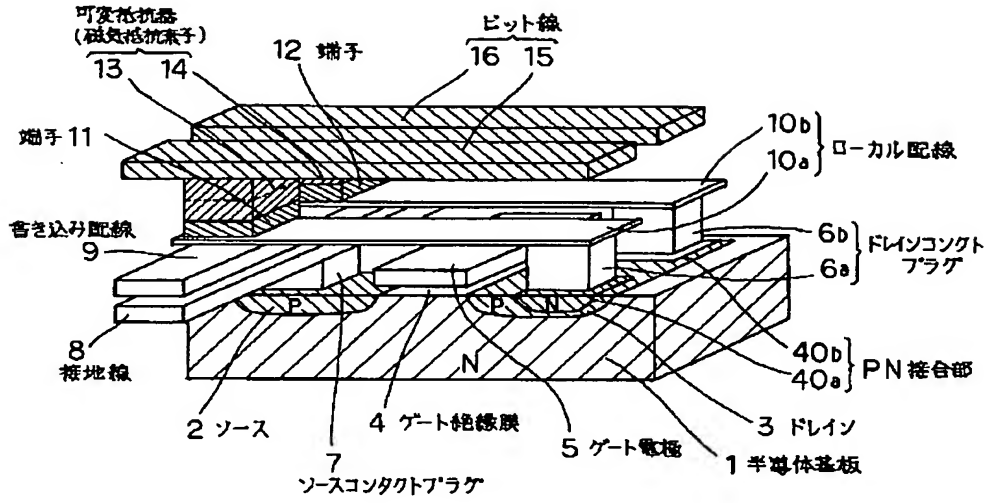
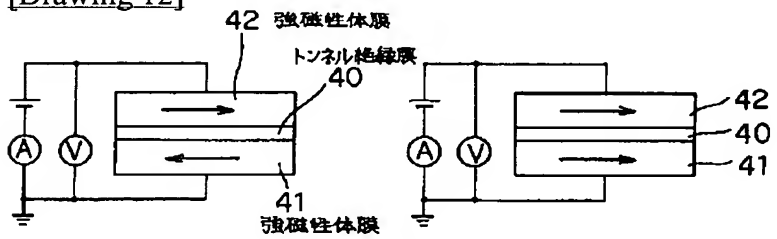


[Drawing 9]

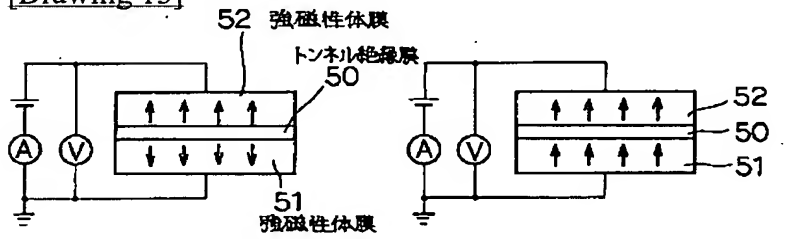


[Drawing 12]



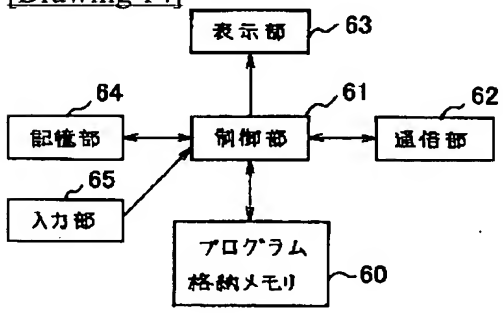
(a) 抵抗大 (b) 抵抗小

[Drawing 13]

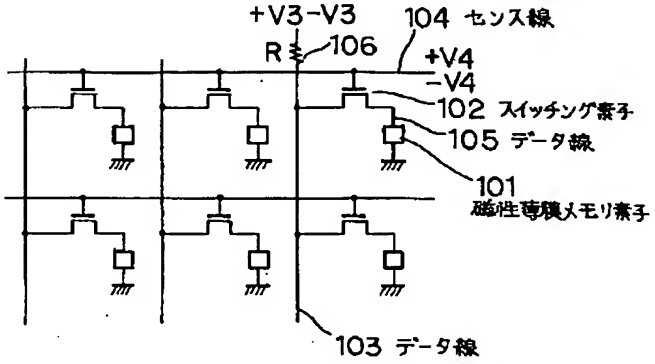


(a) 抵抗大 (b) 抵抗小

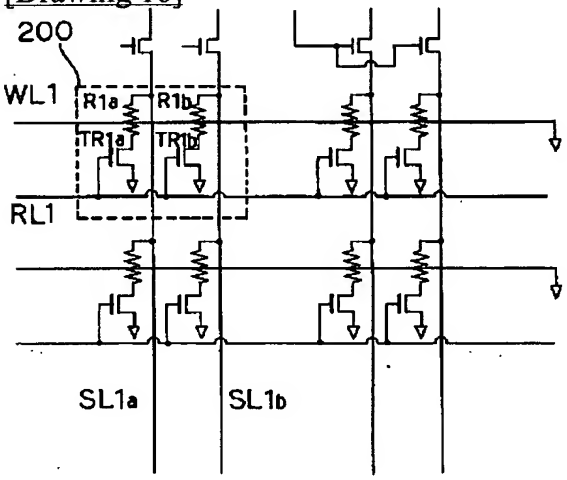
[Drawing 14]



[Drawing 15]



[Drawing 16]



[Translation done.]